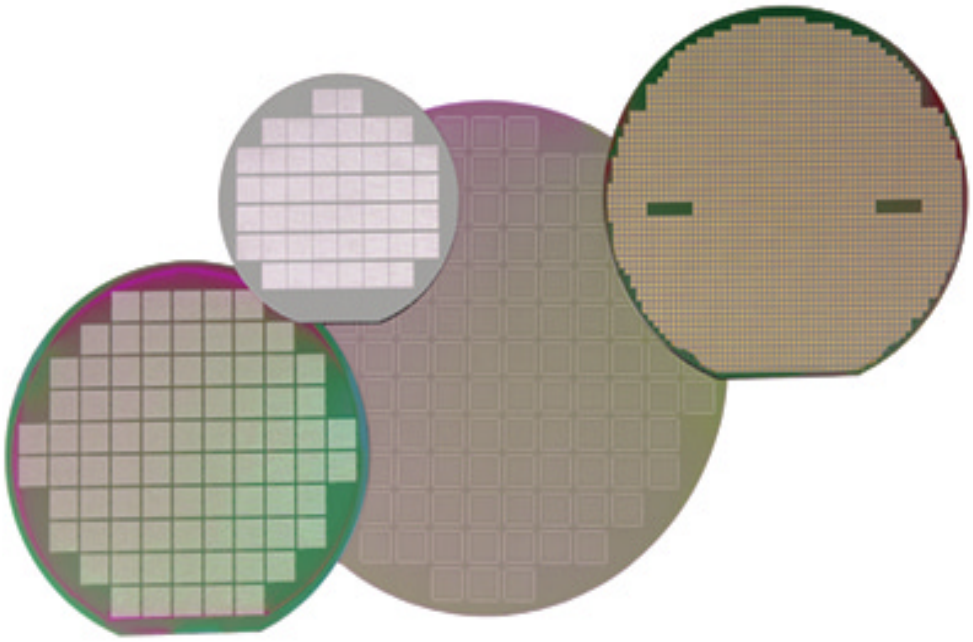
Kulicke & Soffa

Flip Chip Division



Standard Flip Chip Design Guide

Bump Design Guide

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1. INTRODUCTION

This Design standard reviews the design requirements for Kulicke & Soffa's Flip Chip Division's (FCD) standard bumping process. This standard bumping process, also referred to as Flex-on-Cap (FOC), involves the use of FCD's low stress Al/NiV/Cu thin film Under Bump Metallurgy (UBM) and solder application technology. These design rules will be applicable for both eutectic 63Sn/37Pb solder, low alpha eutectic 63Sn/37Pb solder, and high lead 90Pb/10Sn solder.

2. GENERAL DESIGN REQUIREMENTS

2.1 Scribe Line - The scribe line requirements are strongly dependent on the customer's wafer saw capability. The information provided as part of this design standard will be based on the distance from the center of the IC bond pad to the edge of the die. This requirement is based on FCD process requirements and will provide adequate bump clearance for wafer saw. The actual street width will be customer dependent and passivation in the scribe is not required but is preferred.

2.2 Passivation Types - Wafer passivation can be nitride, oxynitride, or polyimide. Polyimide coated wafers should be evaluated for compatibility to the FCD bumping process. Since so many variations of polyimide are available in the IC industry, the customer should provide a scrap wafer to understand the potential impact.

2.3 Fusible Links - Any passivation openings that expose underlying IC metalization are susceptible to attack by the etch processes employed in the FCD bumping processes. If openings exist such as fusible links, they must have passivation protection or the exposed metalization will be attacked.

2.4 Passivation Openings Without Solder - Passivation openings such as test patterns can be protected with UBM with no solder applied. The UBM will be square or rectangular so it is not confused with the circular UBM structures that receive solder. The non-soldered UBM should overlap the passivation opening by a minimum of 7µm each side. The minimum distance between non-soldered UBM pads should be 15µm.

2.5 UBM Type and Dimensions - The UBM utilized by FCD is comprised of sputtered layers of Al, NiV, and Cu. The FCD bumping process has been optimized using this metallurgy. The UBM system is sometimes called a pad limiting metal (PLM) or ball limiting metal (BLM) in other bumping processes. UBM sizes receiving solder shall be the same size. The size of the UBM that does not receive solder can vary but must protect the intended passivation opening.

2.6 Wafer Sizes and Thickness - Wafer sizes of 6-inch (150mm) and 8-inch (200mm) are accepted for bump processing. Minimum acceptable wafer thicknesses for standard wafer bumping are 18mils (457um) for 150mm wafers

and 22mils (560um) for 200mm wafers.

2.7 Probed Wafers and Ink Dots - Wafers must not contain ink dots but probe marks on IC bond pads are acceptable.

2.8 Customer Data Requirements - The following data are required from each customer in order for FCD to successfully complete a bump design

2.8.1 Accurately completed Mask Design Information Form (MDIF). This form can be found at the end of this document.

2.8.2 Electronic copy of GDSII file with only the final metal and final passivation layers.

2.8.3 Wafer shot map (or scrap wafer where possible) showing array of die on wafer.

2.8.4 Purchase Order.

3. SOLDER TYPES

FCD offers a variety of solder types to meet customer specific requirements. Although standard solders are high lead and eutectic, FCD is not limited to binary solder alloys and development of lead free and ultra low alpha solders to meet market requirements are ongoing. Contact a FCD Product Engineer for specific information on solder types.

3.1 Eutectic 63Sn/37Pb Solder - This is the most widely used solder for computer, communications, and other consumer electronics. Eutectic 63Sn/37Pb solder has a eutectic point at 183 ^{0}C, and typical peak reflow temperatures between 220 and 240 ^{0}C are used. The typical collapse of the eutectic solder during assembly is between 25% and 35% of the bump height prior to assembly. The amount of collapse is directly dependent on the substrate land area. Recommended substrate land areas are 100% to 125% of the area of the bump UBM.

3.2 Low Alpha Eutectic 63Sn/37Pb Solder - Low alpha eutectic solder is the same solder type as the FCD standard eutectic with the exception of the high purity lead utilized to make the solder. The use of low alpha lead and controlled solder paste preparation methods result in alpha particle emissions below 0.02 counts/cm^2/hr.

3.3 Ultra Low Alpha Eutectic 63Sn/37Pb Solder – This eutectic solder is alloyed with even higher purity lead for applications with extreme sensitivity to alpha particles. The alpha particle emission for this solder is below 0.002 counts/cm^2/hr.

3.4 High Lead 90Pb/10Sn Solder - For applications requiring higher melting temperature solders, FCD provides a 90Pb/10Sn solder. This solder, which has

a melting temperature of 318^{0}C and typical peak reflow temperatures between 330^{0}C and 340^{0}C, provides the same reliability and applicability as other high

lead solder alloys such as 95Pb/5Sn. The high lead solder can be employed for applications with higher power or current density requirements.

4. DESIGN CONSIDERATIONS

FCD design rules are established for standard bump pitches processed regularly at FCD. The basic design requirements for these rules are based on the size of the UBM and the required solder bump height. It is important that these standards are followed to produce a robust, manufacturable bump.

4.1 UBM Design Requirements – One basic design requirement is the size of the UBM in relation to the sizes of the IC metal bond pad and the passivation opening. These dimensions correlate to the IC bond pad pitch. The UBM size and device pitch determine the possible bump height for the device. Figure 1 shows the dimensional requirements for the UBM in relation to the passivation opening and the IC metal bond pad. This design scheme ensures a reliable, robust bump in several ways. The overlap of the UBM to the passivation opening provides a seal to the underlying IC aluminum bond pad. This overlap shall be a minimum of 10um on each side of the UBM. The containment of the UBM inside the IC metal bond pad eliminates stresses that can cause silicon cratering. This dimension is 6 µm on each side of the UBM.

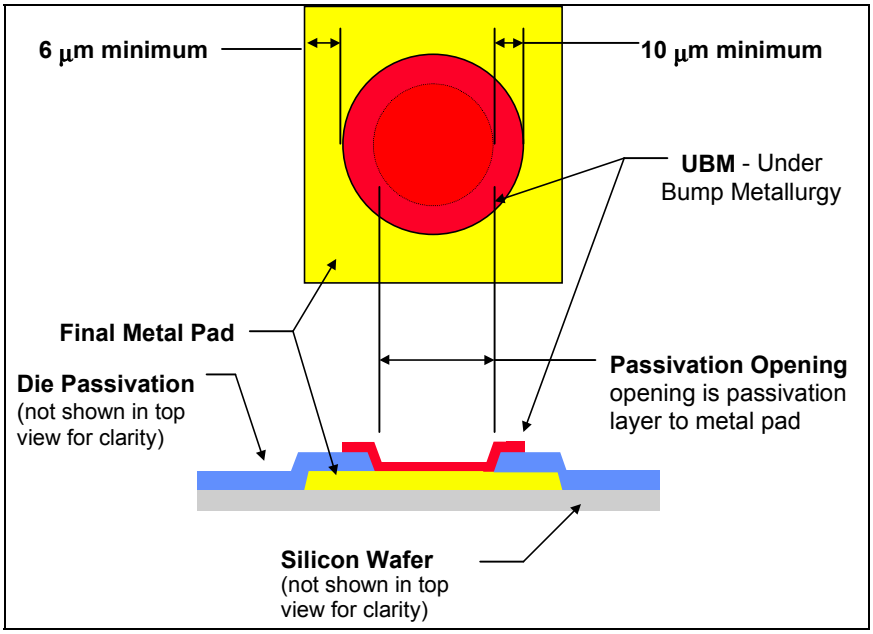

Figure 1. Dimensional requirements for solder bump UBM.

4.2 Solder Bump Height Design Requirements - The solder bump height is established to provide sufficient solder volume to obtain the required standoff

after flip chip mounting on a substrate. The solder bump height is dependent on the pitch of the device and the required UBM dimension. As described earlier, the various design factors such as final metal bond pad size, passivation opening, UBM diameter, and device pitch need to be correlated to ensure a robust bump design. Tables 1 and 2 identify the design requirements based on device pitch for peripheral and array layouts, respectively; devices with more than one peripheral row should use the array design rules. In addition, the pitch between bumps on adjacent devices must be considered. If there are questions on how to optimize a solder bump design, please contact a FCD Product Engineer.

Table 1. Peripheral Solder Bump Design Guidelines.

Peripheral Pitch	**254 (10mil)**	**204 (8mil)**	**152 (6mil)**	**127 (5mil)**
UBM Mask Name	Cap6	Cap4	Cap3.5	Cap3
UBM Diameter	152	102	90	75
Max Passivation Opening Diameter	132	82	70	55
Minimum Final Metal Size	164	114	102	87
Approved for Sn63/Pb37	YES	YES	YES	YES
Approved for Pb90/Sn10	YES	YES	NO	NO
Bump Height Mean	130	100	87	75

All dimensions are microns unless noted.

Table 2. Solder Bump Array Design Guidelines.

Array Pitch	**254 (10mil)**	**227 (9mil)**	**204 (8mil)**	**177 (7mil)**	**160 (6.3mil)**
UBM Mask Name	Cap4	Cap3.5	Cap3.2	Cap3.2	Cap3
UBM Diameter	102	90	80	80	77
Max Passivation Opening Diameter	82	70	60	60	57
Minimum Final Metal Size	114	102	92	92	89
Approved for Sn63/Pb37	YES	YES	YES	YES	YES
Approved for Pb90/Sn10	YES	YES	NO	NO	NO
Bump Height Mean	105	100	90	78	75

All dimensions are microns unless noted.

4.3 Corner Bumps - Corner bumps are the bumps in the far edge of the die which create the maximum distance from neutral point (DNP) and therefore should be eliminated. If a corner bump is required, the design rules used will follow array design requirements since the corner bump and the two adjacent bumps within the row create an array area. The minimum pitch for the design will be the minimum distance between the centers of any two bumps.

5. ALIGNMENT AND TOLERANCES

Please see FCD's "Alignment Design Guide" on our website www.flipchip.com.

6. MAXIMUM JUNCTION TEMPERATURES AND CURRENT

Reliable flip chip operation is a function of the mechanical assembly (i.e., construction, underfill adhesion, etc.), board technology, current density, temperature of operation, etc. The design rules in this section are specifically designed to assure the integrity of the solder bump and the UBM. The two failure modes that these design rules cover are the electromigration of the 63Sn/Pb solder and the consumption of the Ni barrier layer that is part of the FCD UBM. Extrapolations of these design rules should not be attempted for other UBM or solder alloy systems.

6.1 Average Bump Temperature - The average bump temperature is important for electromigration and the UBM Ni consumption. The average bump temperature is typically less than the junction temperature of the device but is dependent upon the cooling solution used and the ambient conditions. In general if the average bump temperature is not known it is better to bias the temperature used in the analysis towards the chip junction temperature.

6.2 Electromigration - The electromigration of the 63Sn/Pb solder in the flip chip bump is a function of the current density and the average bump temperature. Electromigration is the dominant failure mechanism at higher current densities for a given temperature. In the design rules provided, the solder electromigration projected first failure has been calculated based on the calculated Weibull life and slope of 4 and a calculated first failure at 0.9%. This value has been multiplied by 0.8 as an additional safety factor. Figure 2 shows an example of solder migration in the direction of electron flow. Note that the actual solder separation is often not very discernible. The large gap shown in Figure 2(a) actually occurred during cross sectioning and SEM analysis when some of the solder fell away along the solder migration line. When observing SEM cross sections of bumps that fail because of electromigration, a segregation of the Sn (dark) and Pb (light) start to form. In Figure 2, you can observe the segregation of the eutectic into distinct areas within the bump.

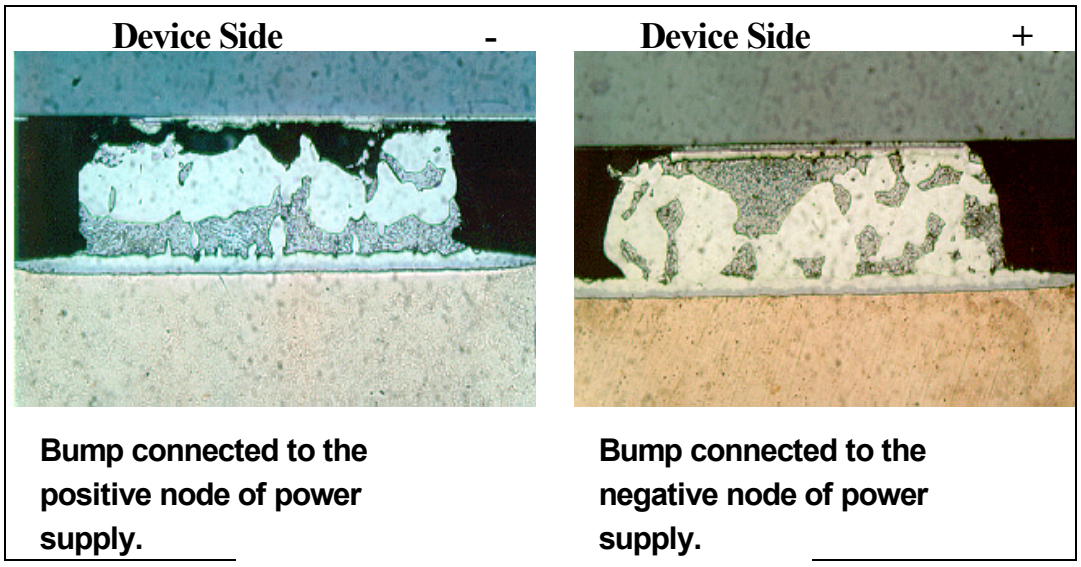

Figure 2. Electromigration Failure Cross Section

6.3 UBM Ni Consumption - The consumption of the Ni barrier layer in the UBM is a function of the average bump temperature, the current density and the amount of Au present in the solder joint. The Ni consumption failure has been defined as an exposure of 5% of the Al bond pad..

6.4 HTOL Testing - HTOL (High Temp Operating Life) testing is an accelerated test that stresses the chip assembly with a current density and temperature that is greater than operating conditions. The primary failure mechanism this will uncover in a flip chip application is the electromigration of the solder and the consumption of the UBM. Typically, the HTOL testing is done with a chip that is heated to a junction temperature (T_j) that is 20 to 40 degrees greater than the ambient temperature (T_a). In the design rules a recommended set of maximum conditions will be specified for HTOL testing.

It is extremely important during HTOL testing that the temperature of the chip and the ambient temperature be well controlled. This requires either the mounting of thermocouples to the chip or accurate calibration of the temperature sensing diode used on the chip. Lessons have been learned that the design of the sensing diode may not be the same from part number to part number even in the same family, resulting in temperature sensing errors of 15-25C. It is therefore critical that every chip used for HTOL testing be calibrated.

During HTOL testing the average solder bump temperature will be a function of the junction temperature, the board temperature, airflow in the chamber, cooling solution, etc. As FCD has no control over these test condition variables the value specified for HTOL testing assumes that the average bump temperature is

equal to the junction temperature. If it is known that the average bump temperature will be less than the junction temperature and a higher current or junction temperature is required for HTOL testing please contact your FCD's Product Engineer.

6.5 HTS Testing - HTS (High Temp Storage) testing is an accelerated test that stresses the chip assembly with a temperature that is greater than operating conditions. The primary failure mechanism this will uncover in a flip chip application is the consumption of the UBM. Typically the HTS testing is done with an un-powered chip in a heated test chamber. In the design rules a recommended set of maximum conditions will be specified for HTOL testing.

6.6 Board Technology - The pad construction on the board has a significant effect on the reliability of the flip chip solder bump. A pad which has no Au provides the most reliable bump technology. For many board or substrate technologies however the presence of Au on the pad is required. In these board technologies it is recommended to limit the amount of Au present. The amount of Au present is a function of both the Au thickness and the amount of solder wicking under the solder mask on the board. It is recommended to keep the Au thickness ≤ 0.2microns for the best reliability. If the Au thickness is nominally > 0.2microns please contact your FCD's Product Engineer for assistance.

For laminate board technologies that utilize electroless Ni and Au finishes the plating can either be done before solder mask application or after solder mask application. Solder masks that are applied after the electroless Ni and Au plating often have difficulty adhering to the Au finish. When the solder mask loses adhesion to the Au finish solder wicking occurs underneath the solder mask and more Au is incorporated into the solder bump. Preferably the electroless Ni and Au plating will be done after the solder mask application to limit the amount of Au in the solder joint, this type of construction is called "selective plating".

The values provided in the following sections assume that the solder mask will lift and additional Au will be incorporated in the solder joint. The construction with solder mask over the electroless Ni and Au finish is called "non-selective plating". If it is known and absolutely repeatable that wicking does not occur in a "non-selective plating" construction it is permissible to utilize the "selective plating" values. Data for selective Au plating of 0.7microns thickness on the pad is equivalent to a poor solder mask with severe solder wicking.

6.7 Safe Current and Max T_j Design Rules - The following design rules are a guide for design requirements for electromigration and UBM consumption. The maximum T_j that the solder bump can withstand for UBM consumption is based on

the substrate pad finish. If no gold is used for the pad finish, the maximum T_j is 150 C. If a substrate pad finish includes a gold finish, the maximum T_j is

identified in Table 5. This maximum T_j takes precedent over the electromigration requirements and dictates the maximum allowable junction temperature.

Once the maximum allowable T_j for the substrate pad finish is identified, then the maximum current (milliamps) per bump for electromigration can be evaluated. The electromigration mean time to failure (MTTF) is based on 10,000 hours and is specific to UBM diameter and device passivation via diameter in relation to device junction temperature. Table 6 shows the maximum current carrying capability per bump in milliamps for a specific passivation opening diameter and required T_j based on the assumptions in Section 6.2 Again the T_j should not exceed the T_j identified in Table 5 for UBM consumption.

Design requirements that exceed the values in Table 5 and Table 6 should be reviewed with a FCD Product Engineer to ensure application specific requirements can be met. Please note that higher max T_j performance can be obtained with FCD's Pb90/Sn10 solder when substrate requirements dictate gold finishes. Recommended test conditions for High Temperature Operating Life (HTOL) or High Temperature Operating Bias (HTOB) are shown in Table 7.

Table 5. Maximum T_j for substrate pad performance using eutectic Sn63/Pb37 solder.

PWB CAPTURE PAD	Max Tj
Cu OSP, PdAg or PtAg	150
Selective Au/Ni	140
Non-selective Au/Ni	130

Table 6. Maximum eutectic Sn63/Pb37 solder bump current carrying capability for MTTF = 10,000 Hrs. Cap number is the UBM size in mils and the via size is the diameter of the device passivation opening in mils.

Junct Temp	Cap6/Via5.0	Cap4.7/Via3.8	Cap4.0/Via3.1
	MilliAmps	MilliAmps	MilliAmps
150C	120	70	45
140C	160	92	60
130C	220	126	82
120C	305	170	115

Table 7. Recommended test conditions for HTOL/HTOB

Test Conditions

1000 hours
Tamb of 125C
Tj of 150C
0.15 microns of selective Au
80 micron passivation opening
Acceptance Criteria
0 fails in 76 piece sample
1 fail in 129 piece sample
FCT Design Rule to Meet HTOL/HTOB Test
Amps assuming average bump temperature of 145C is achieved during test

7. SUBSTRATE DESIGN

Substrate design for flip chip has been a challenge especially for fine pitch flip chip applications. Design trade-offs are commonly found to accommodate manufacturability and cost by compromising package reliability. Typical board manufacturers consider 3 mil line/space as an advanced process, while 2 mil line/space is still considered to be leading edge technology. A solder mask registration tolerance of ± 2 mils is considered an advanced process while the comfort zone lies in 2½ - 3+ mil range. Typically a minimum web of 3 mils is required to allow proper adhesion of a solder mask to the laminate base material.

The creation of a solderable pad is the most important aspect of the design. Pads must be designed with consideration of the board house capabilities, bump size, effect on assembly yield and reliability. By design, the data shows that a bump height should be kept as high as possible, so therefore, the pad site should be designed in such a manner that the solder maintains the original bump shape. If the PCB pad is the same size as the dice pad, this scenario would be optimum. The difficulty with this concept lies in the accurate creation of this pad site on the PCB. Consider a dice with an 8 mil bump pitch. This dice will have a bump that is in the 4 - 5mil height range and 4.5 - 6 mil bump diameter. The dice will have a pad dimension that is approximately 4½ mils. The creation of a 4½ mil pad on a laminate PCB is outside the capability of most board shops. The difficulty lies in the tools that they use for manufacturing standard PCBs, for which the dimensional tolerances are much greater.

The wettable area of the substrate pad, along with the solder bump volume and UBM pad size, determines the final solder joint shape. A high standoff and a near 1:1 UBM/Cu Pad ratio is desired from a reliability stand point. However, the ideal solder geometry is not always achievable because of board manufacturability considerations. This is especially true for fine pitch flip chip applications. Pad/UBM ratio is usually 125%, 150% and even higher, in order to accommodate tolerances in solder mask registration and die placement. As a

result, the bump standoff is lower which not only creates problems for the underfill process, but may also result in reduced reliability.

There are two ways of defining the solder wettable area: solder mask defined (SMD) or non-solder mask defined (NSMD). The NSMD pad is also called etch-defined (or copper-defined) pad. The solder bump can only wet to the top surface of SMD pads defined by the solder mask, while a NSMD pad allows solder to wet the side wall of the pad. For flip chip applications, SMD pad design is not always possible on pitches of less than .010 inches due to dimensional limitations. The pad and capture pad sizes are limited by bump pitch, routing, solder mask registration, and minimum solder mask web. However, a partial NSMD design can be used. A revised design uses partially non-solder mask defined pads and allows the solder mask registration below ± 2 mils and also allows the board fabrication to be done in a larger panel. Building boards on a larger panel can significantly reduce the fabrication cost. The trace thickness was specified at ¼ oz Cu, which can improve dimensional accuracy in metal etch and also increase the effective bump standoff. A thin solder mask is also desired to accommodate subsequent underfill processes.

For partial NSMD pads, it is important to have a thin Cu trace, since the solder wets over the sides. A thick Cu trace (1/2 oz Cu plated up to an equivalent of nearly 2 oz) which not only reduces the effective bump standoff, but also creates problems for underfill. The thick conductor trace also results in a more rigid solder bump structure and thus compromises flip chip reliability. A thinner Cu trace (1/4 oz) and solder mask, along with a modified underfilling process, significantly improves the quality of underfill. The copper conductor is typically etched from a copper clad laminate. Common Cu weights, or thickness' range from 1 oz (1.4 mils) to ½ oz (0.7 mils), or even ¼ oz (0.3 -0.4 mils). For coarser pitch devices (> 18 mils pitch, CSP, BGA etc.), 1/2 - 1oz Cu is suitable to use because the bumps are normally higher than those in finer pitch devices. For fine pitch devices (e.g. 8 or 10 mil pitch), a thinner Cu layer is desired. However, consideration must be given to the final copper thickness, since during processing the plating of through holes adds to the trace thickness. There are several options for conductor finishes: Cu with OSP finish or Ni/Au finish. CuOSP is the preferred conductor finish but Ni/Au finish is also commonly used in flip chip packages. A typical specification is for electroless nickel of 100 to 200 µinches and an immersion gold finish of 5 - 8 µinches. If the gold layer is too thick, the solder joint may fail early due to electromigration or UBM consumption as described earlier. If the gold layer is too thin, poor wetting may occur during the assembly process due to Au porosity and nickel oxidation. Whenever copper is used, an oxidation protection layer is needed because copper will readily oxidize in air. The use of an organic surface protection (OSP) not only lowers the cost in board manufacturing process, but also eliminates the gold impact.

8.0 GLOSSARY OF TERMS

Array Pattern Number of rows and columns in the in a matrix-designed layout of solder balls.

Bump Diameter	The widest measurement through the center cross-section of a re-flowed bump.
Bump Height	Vertical measurement from the top of the UBM to the top of the bump after reflow. (not yet attached to PCB substrate. After assembly, the analogous measurement is called "stand-off height".)
Bump Shear	Shear value and failure mode during shear test with standard offset from the die surface and shear speed.
Bump Standoff Height	Measurement from substrate surface to silicon surface
Cu Pad	Solder receiving pad on the substrate that is Cu etch-defined.
Die size	The silicon area bounded on the outside by the scribe street.
DNP	Distance to neutral point. The distance from an I/O to the center of mass of the die. Maximum DNP defines the largest array size for a given process technology that will meet the minimum thermal fatigue performance criteria as established by FCD.
I/O	The location of the signal interface that contacts to the "outside" world. Also called the "bump location" (formerly "bond pad" in the context of molded/leaded packages).
IC metal pad size	Size of metal bond pad on IC, as manufactured during normal IC processing.
OSP	Organic Surface Protectant used to prevent copper traces on printed circuit boards from oxidation. It is the preferred pad finish on circuit boards.
Pitch	The linear distance between two adjacent I/Os or bump locations.
PCB	Printed Circuit Board.
PO	Passivation Opening at the I/O bond pads.
Solder Mask	A layer of organic material covered on top of outer-layer conductor (Cu) that has openings to allow solder wet to the Cu pads and prevent solder bridging in the rest area. These openings are called Solder Mask Openings.

Stepping Distance Linear measurements in both the x and y directions comprising die size and to the center of the scribe streets on all four sides.

UBM Under-Bump-Metallurgy. The metal stacks deposited on the IC bond pad forming the base of the solder bump. The UBM is also referred to as the pad limiting or bump limiting metal. It has the combined features of adhesion layer, diffusion barrier, wetting layer and oxidation protection layer.